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SIMULATION OF THE EFFECT OF A SINGLE INTERFACE TRAPPED CHARGE IN FINFET WITH A GATE LENGTH OF 10 NM ON THE SHORT CHANNEL EFFECTS

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Rezume. Maqolada kanal uzunligi 10 nm izolyatsiyalangan zatvorli vertikal maydoniy tranzistorning oksid-yarimo`tkazgich chegara sirtida qamralgan yakka zaryadning SS va DIBL effektlariga ta`siri modellashtirish orqali o`rganilgan. Bunda chegara sirtida qamralgan zaryadning kanal tomi va yon sirti o`rtasida joylashgan vaziyati L_{gx} ga bog`liq holda SS va DIBL ning o`zgarishlari hisoblangan.
**Kalit so`zlar:** Vertikal MOY transistor, MOY transistor, qisqa kanal effektlari, qaralgam yakka zaryad, potentsial,oksid-yarimo`tkazgich qatlam, stok tomonidan potensial to`siqni kamayishi (DIBL)
Аннотация. В статье рассматривается влияние единичного заряда, встроенного на верхней и боковой поверхности канала FinFET транзистора на такие короткоканальные эффекты (DIBLэффект и SS). Исследуется зависимость указанного влияния от положения заряда на верней и боковой поверхности вдоль канала.
Ключевые слова: Вертикаль МОПТ, МОПТ, короткоканальные эффекты, пойманный в ловушку один заряд, потенциал, оксидно-полупроводниковый слой, Слив-индуцированного барьера снижение (DIBL)
Abstract. In the article, the effect of a single charge on the surface of the oxide-semiconductor boundary of a vertical field-effect transistor with an isolated gate length of 10 nm is studied by modeling the effects of SS and DIBL. In this case, the change in SS and DIBL depending on the position L_{gx} of the charge on the surface of the boundary, located between the roof of the channel and the side surface.
Key words: FinFET, MOSFET, short-channel effects, trapped a single charge, potential, oxide-semiconductor layer, Drain-induced barrier lowering (DIBL)

Introduction. In 1965, Gordon Moore, one of the founders of Intel, discovered that two years after the advent of new chip models, the number of transistors in them had almost doubled each time. He predicted that by 1975 the number of elements in the chip would be 2^5 times higher than in 1965. [1]

He concluded that if this trend continues, the performance of computing devices could grow significantly in a relatively short period of time. This observation is later called Moore's Law. Moore's law continues in almost the same direction to this day. As a result, the number of transistors on each chip increases and their geometric

dimensions decrease. However, the reduction in the geometric dimensions of the transistors on the chip causes them to have various degradation effects, including short-channel effects. Reducing such degradation effects in nanoscale transistors is one of the most pressing issues in nanoelectronics.

This article is about one of the most important issues in nanoelectronics. The effect of SS (subthreshold swing) and DIBL (Drain-induced barrier lowering), one of the short-channel effects that occur in nanoscale vertical field-effect transistors, is the effect of a single charge on a defect at the boundary surface of an oxide-semiconductor layer using Sentaurus TCAD studied through modeling.

Methodology calculating of DIBL and SS. The DIBL effect is mainly a short-circuit effect on the surface of nanoscale transistors. Its physical meaning is as follows: how much does the voltage across the transistor stock Vd change when the transistor threshold voltage changes by one unit, i.e.

$$DIBL = \frac{\Delta V_{th}}{\Delta V_d} = \frac{V_{th2}(V_{d2}) - V_{th1}(V_{d1})}{V_{d2} - V_{d2}},$$

here,

V_{d1}- it is the low current voltage applied between the stock and supply fields.

V_{d2}- it is the high current voltage applied between the stock and demand fields.

$V_{th1}(V_{d1})$- it is the threshold voltage corresponding to the low current Vd1 applied between the stock and supply fields.

$V_{th2}(V_{d2})$ - it is the threshold voltage corresponding to the high current Vd2 applied between the stock and supply fields.

When calculating the various parameters of FinFET, it is necessary to determine the threshold voltage. Threshold voltage V_{th} is defined as the gate voltage corresponding to the threshold current of the transient volt-ampere characteristic.

For nano-sized FinFET transistors, the threshold current is found using the following formula using the geometric dimensions of the transistor.

$$I_{th} = \frac{W_{eff}}{L_g} \cdot 2 \cdot 10^{-7}\ [A],$$

where Lg is the gate length, the effective width of the W_{eff} transistor channel, and in three-gate transistors it is calculated as follows.

$$W_{eff} = 2 \cdot T_{si} + W_b,$$

where T_{si} is the height of the transistor channel layer, W_b is the width of the transistor channel layer, and L_g is the length of the transistor channel.

Short-channel effects include, in addition to the DIBL effect, a decrease in the verticality of the transition characteristic. Typically, to evaluate the effect of such a short channel, the magnitude inverse of the verticality of the transition volt-ampere characteristic in the area below the threshold is considered and is denoted by SS (Subthreshold swing).

The magnitude of SS is the inverse of the slope of the field below the threshold voltage, and its calculation formula is:

$$SS = \frac{\Delta V_g}{\Delta lg I_d} = \frac{V_{th} - (V_{th} - 0{,}2)}{lg I_{th} - lg I_{off}} = \frac{0{,}2}{\lg(\frac{I_{th}}{I_{off}})} \qquad [\frac{mV}{dec}],$$

where ΔV_g - is the difference between the threshold voltage V_{th} and the gate voltage corresponding to the closed state of the transistor. In our study, a voltage less than 200 mV was obtained from the threshold voltage as the gate voltage corresponding to the closed state of the transistor. ΔlgI_d is the difference of the I_{off} current corresponding to the closed state of the threshold I_{th} corresponding to the threshold voltage.

Simulation procedure and FinFET structure. The classical diffusion-drift physics model was used to model the transistor under study. This model uses the following Poisson and continuity equations:

$$\nabla\, \varepsilon\nabla\varphi = -\, q\,(p - n + N_D\, - N_A\,) - \rho_{trap}\,,$$

where $\boldsymbol{\varepsilon}$ – it is the dielectric constant, q – it is the electron charge, p – and n – these are the concentration of electrons and poplars respectively, N_D– and N_A– these are the concentration of ionized donors and acceptors respectively, ρ_{trap}– it is the charge on the defect, and charge density generated from fixed charges. The continuity equation is given by:

$$\nabla \cdot J_n\, = qR_{net}\, + q\,\partial n\,/\partial t\,;$$
$$-\nabla\, J_p\, = qR_{net}\, + q\,\partial p\,/\partial t\,,$$

where J_n – and J_p – these are current density for electrons and poplars respectively, R_{net} – it is electron-poplar recombination rate. The current density for electrons and poplars is determined by the following expressions:

$$J_n\, = -nq\mu_n\,\nabla\Phi_n\,; \qquad J_p\, = -pq\mu_p\,\nabla\Phi_p\,,$$

where Φ_n – and Φ_p – these are the quasi Fermi potential of the electron and the poplar respectively, μ_n – and μ_p – the mobility of the electron and the poplar [7-13].

This requires quantum effects to be taken into account in the modeling because the transistor being modeled is in nanometer sizes outside the classical diffusion-drift physical model used. To account for the quantum effects, the quantum correction Λ_n is included in the expression n of the current carrier density:

$$n = N_c F_{\frac{1}{2}}\left(\frac{E_{F,n} - E_c - \Lambda_n}{kT_n}\right)$$

The quantum correction Λ_n expression is based on the density gradient model commonly used in FinFET transistors and has the following form:

$$\Lambda_n = \frac{\gamma\hbar^2\nabla^2\sqrt{n}}{6m_n\sqrt{n}}\,,$$

where γ - is the convergence factor, m_n - is the electron mass.

The transition based on the applied model is given in the voltammeter characteristic [2], calibrated by experimental results. In this case, the transistor parameters were selected in accordance with the production technology as follows: L_{gate}=10 nm in length of the silicon substrate (G), HfO_2 with equivalent thickness t_{ox}=0.35 nm as the substrate oxide layer, the length and width of the substrate oxide layer, respectively, L_{box} = 30 nm and W_{box} = 100 nm [3].

The width W_t of the roof is taken as a parameter to represent the shape of the channel, and varies between 5 nm for a trapezoidal channel and 10 nm for a rectangular channel. The transistor channel is alloyed with boron up to a concentration level of 10^{15} sm^{-3}, the width of its base is W_{fin} = 10 nm, and the stock areas are alloyed according to

the Gaussian distribution with phosphorus with a maximum concentration of 10^{20} sm^{-3}. The length of the istok and stock fields is 10 nm. The radius of the field charged with a single charge (single electron charge) covered at the oxide-semiconductor boundary is 0.5 nm, and the charge density is $1.27 \cdot 10^{14}$ sm^{-2}. In modeling, the charged field is modeled with a uniformly charged circle. The radius of the circle is close to the distance between the atoms, which is typical for crystalline silicon, ie 0.543 nm [4-6]. The structure of this modeled transistor is shown in Figure 1.

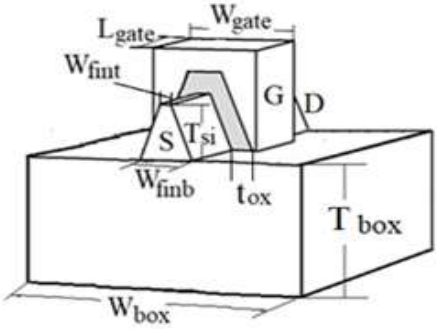

Figure 1. The geometric structure of the modeled vertical field-effect transistor

Results and Discussions. In this case, the position of the single charge covered at the oxide-semiconductor boundary of the vertical field-effect transistor depends on the two positions (between the roof and the side of the channel) and the cross-sectional shape of the channel (rectangular and trapezoidal). The effects on the DIBL effect and SS were modeled. For the SS and DIBL effect, the L_{gx}-dependent change in the position of the single charge channel along the channel between the roof and side surfaces of the single charge channel covered at the oxide-semiconductor boundary was calculated by modeling. The results obtained are shown in Figures 2-3.

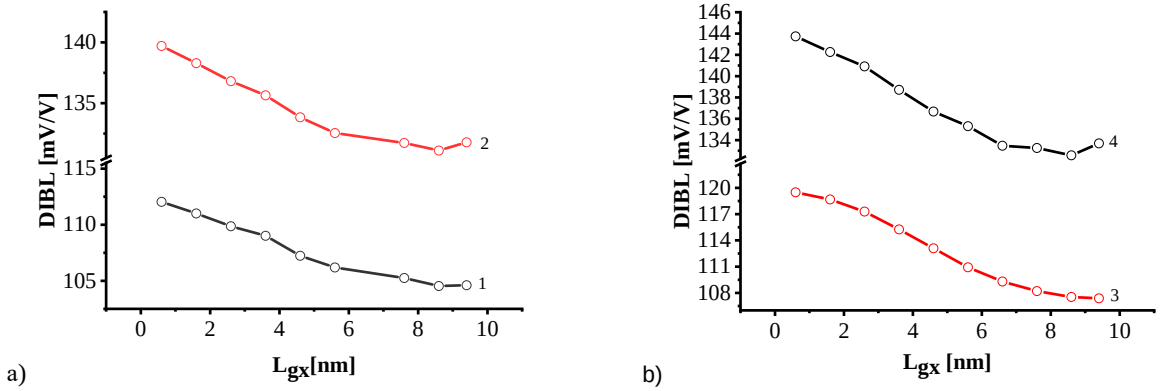

Figure 2. For the two cross-sectional forms of the DIBL effect, the position of the single charge channel covered at the oxide-semiconductor boundary between the roof and the side surface along the channel is related to L_{gx} a) between the roof surface of the covered single charge channel, 1- trapezoidal 2-rectangular cross-sectional transistors b) 3-trapezoidal 4-rectangular cross-section transistors located in the middle of the side surface of the covered single charge channel.

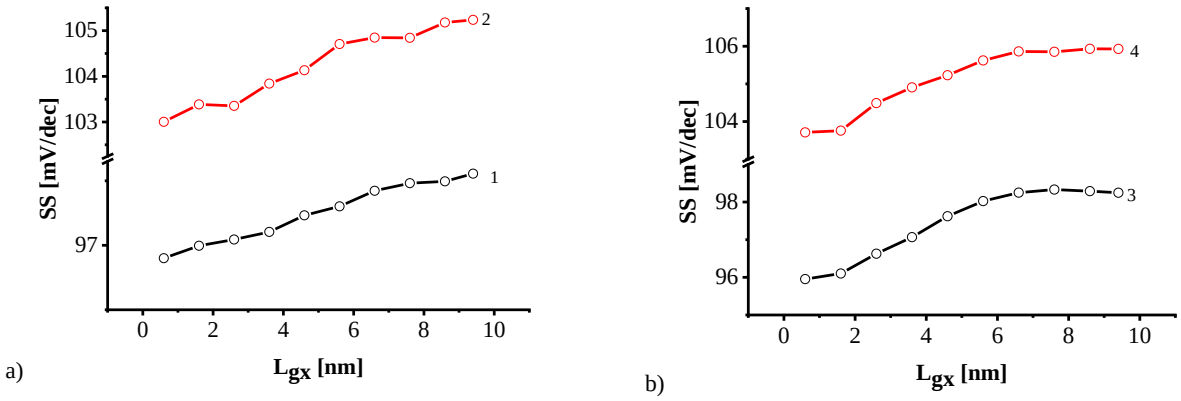

Figure 3. For two cross-sectional forms of SS, the position of the single charge channel covered at the oxide-semiconductor boundary between the roof and the side surface along the channel is related to L_{gx} a) the trapezoid 1 located between the roof surface of the covered single charge channel 2 rectangular cross-section transistors b) 3-trapezoidal 4-rectangular cross-section transistors located in the middle of the side surface of the covered single charge channel.

The results show that in vertical field-effect transistors with a rectangular and trapezoidal channel shape, single charge, when the top surface of the channel of the transistor is covered between the oxide-semiconductor boundary, the SS and DIBL effects are shown to be smaller than when the channel is enclosed between the side surfaces.

With displacement the single trapped charge along the channel from the source side to the drain side the DIBL effect is decreased and SS is increased. Such behavior of DIBL and SS is connected with position of single trapped charge relative point of maximal surface potential. Surface potential distribution (Figure 4) show that point of maximal surface potential is placed at source side relative the center of the channel. When the single charge is trapped at source side DIBL effect is higher and SS is lower than in case when charge is trapped at drain side.

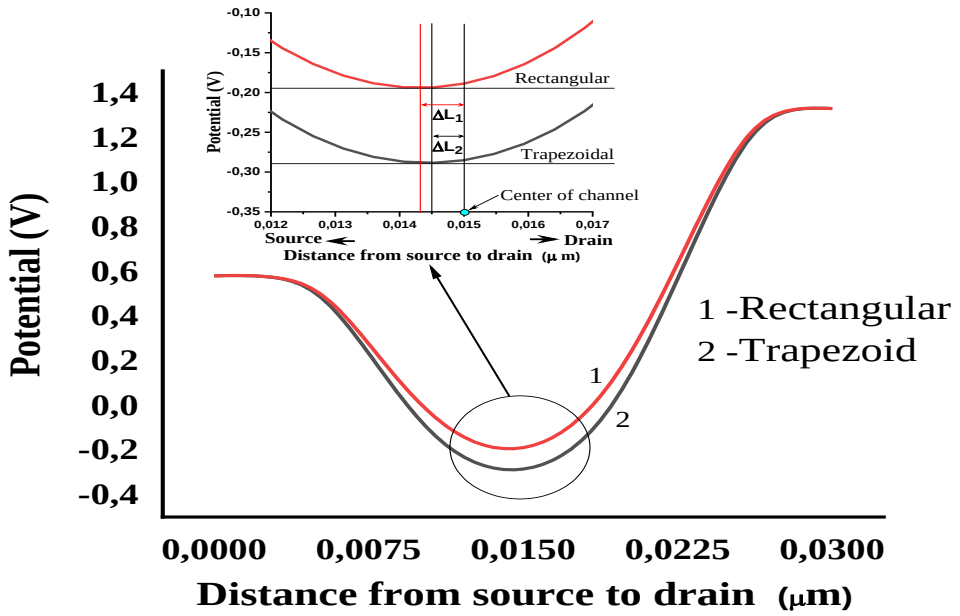

Figure 4. Potential distribution along the channel in FinFET with rectangular (1) and trapezoid (2) channel cross section.

Conclusion. For both types of channel cross-sections, an increase in the DIBL effect and a decrease in SS were found with an approach from the source to the drain of the position of a single charged defect located on the upper and lateral surfaces of the channel. And it was determined that when a single charge is embedded both on the top and on the side surface, the DIBL effect and SS are greater for a transistor with a rectangular cross section than with a trapezoidal cross section.

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